This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently amended) A monolithic structure, comprising:

a first pair of devices and a second pair of devices, each pair of devices comprising:

a first lateral device having a first source terminal, a first drain terminal, and a first gate terminal, each of said first source, first drain, and first gate terminals terminating on a first surface of a semiconductor substrate[[;]], and

a second lateral device having a second source terminal, a second drain terminal and a second gate terminal, each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate, and

a multi-layer metal interconnect structure disposed above each pair of devices,

wherein (i) in each pair of devices, said first drain terminal [[being]]is connected to said second drain terminal via the multi-layer metal interconnect structure, and said first gate terminal [[being]]is connected to said second gate terminal via the multi-layer metal interconnect structure,~~wherein~~ (ii) in each pair of devices, each first lateral device is combined with each second lateral device on said substrate, (iii) both first source terminals are connected to both second source terminals to define a common source terminal disposed in the multi-layer metal interconnect structure of the monolithic structure, and ([[iii]]iv) the multi-layer metal interconnect structure includes a first electrically isolated lead ~~comprises~~comprising the common source terminal.

2. (Cancelled)

3. (Previously presented) The monolithic structure of claim 1 wherein said first and second drain terminals of the first pair of devices are electrically independent of the first and second drain terminals of the second pair of devices.

4. (Previously presented) The monolithic structure of claim 3 wherein said first and second gate terminals of the first pair of devices are electrically independent of the first and second gate terminals of the second pair of devices.

5. (Currently amended) The monolithic structure of claim 3 wherein said first and second gate terminals of the first pair of devices are connected to said first and second drain terminals of the second pair of devices via the multi-layer metal interconnect structure and said first and second gate terminals of the second pair of devices are connected to said first and second drain terminals of the first pair of devices via the multi-layer metal interconnect structure.

6. (Previously presented) The monolithic structure of claim 1 wherein each of said first and second lateral devices comprises a lateral power MOSFET.

7. (Currently amended) A monolithic structure comprising at least four lateral power transistor devices combined on a semiconductor substrate, said monolithic structure comprising:

a first pair of power transistor devices and a second pair of power transistor devices, each pair of power transistor devices comprising:

a first lateral power transistor device comprising a first source terminal, a first drain terminal and a first gate terminal, each of said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate[[;]], and

a second lateral power transistor device comprising a second source terminal, a second drain terminal, and a second gate terminal, each of said second source, second drain, and second gate terminals terminating on said first surface of the semiconductor substrate, and

a multi-layer metal interconnect structure disposed above each pair of devices,

wherein (i) in each pair of devices, said first drain terminal [[being]]is connected to said second drain terminal via the multi-layer metal interconnect structure, and said first gate terminal [[being]]is connected to said second gate terminal via the multi-layer metal interconnect structure, ~~wherein~~ (ii) said first and second gate terminals of the first pair of power transistor devices are connected to said first and second drain terminals of the second pair of power transistor devices via the multi-layer metal interconnect structure, (iii) said first and second gate terminals of the second pair of devices are connected to said first and second drain terminals of the first pair of power transistor devices via the multi-layer metal interconnect structure, ([[iii]]iv) said first and second drain terminals of the first pair of devices are electrically independent of the first and second drain terminals of the second pair of power transistor devices, ([[iv]]v) the multi-layer metal interconnect structure includes a first electrically isolated lead ~~comprises~~comprising both first source terminals connected to both second source terminals, (vi) the multi-layer metal interconnect structure includes a second electrically isolated lead comprises said first and second drain terminals of the first pair of power transistor devices, and (vii) the multi-layer metal interconnect structure includes a third electrically isolated lead ~~comprises~~comprising said second drain terminals of the second pair of transistor devices.

8. (Previously presented) The monolithic structure of claim 7 wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET.

9. (Currently amended) A monolithic structure comprising at least four lateral power transistor devices combined on a semiconductor substrate, said structure comprising:

a first pair of power transistor devices and a second pair of power transistor devices, each pair of power transistor devices comprising:

a first lateral power transistor device comprising a first source terminal, a first drain terminal, and a first gate terminal, each of said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate[[;]], and

a second lateral power transistor device comprising a second source terminal, a second drain terminal, and a second gate terminal, each of said second source, second drain, and second gate terminals terminating on said first surface, and

a multi-layer metal interconnect structure disposed above each pair of devices,

wherein in each pair of devices, said first drain terminal [[being]]is connected to said second drain terminal via the multi-layer metal interconnect structure and said first gate terminal [[being]]is connected to said second gate terminal via the multi-layer metal interconnect structure; ~~wherein~~ and the multi-layer metal interconnect structure includes (i) a first electrically isolated lead ~~comprises~~comprising both first source terminals connected to both second source terminal, (ii) a second electrically isolated lead ~~comprises~~comprising said first and second drain terminals of the first pair of power transistor devices, (iii) a third electrically isolated lead ~~comprises~~comprising said first and second drain terminals of the second pair of power transistor devices, and (iv) a fourth electrically isolated lead ~~comprises~~comprising said first and second gate terminals of the first pair of power transistor devices connected to said first and second gate terminals of the second pair of power transistor devices.

10. (Previously presented) The monolithic structure of claim 9 wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET.

11. (Previously presented) The monolithic structure of claim 9 wherein a size of said second lateral power transistor is smaller than a size of said first lateral power transistor.

12. (Previously presented) The monolithic structure of claim 9 wherein a first threshold voltage of said first lateral power transistor is different from a second threshold voltage of said second lateral power transistor and a difference in said first and second threshold voltages is at least approximately 0.1 V.

13. (Currently amended) A monolithic structure comprising at least four lateral power transistor devices combined on a semiconductor substrate, said structure comprising:

a first pair of power transistor devices and a second pair of power transistor devices, each pair of power transistor devices comprising:

a first lateral power transistor device comprising a first source terminal, a first drain terminal, and a first gate terminal, said first source, first drain, and first gate terminals terminating on a first surface of the semiconductor substrate[[;]], and

a second lateral power transistor device having a second source terminal, a second drain terminal, and a second gate terminal, said second source, second drain, and second gate terminals terminating on said first surface, and

a multi-layer metal interconnect structure disposed above each pair of devices,

wherein (i) in each pair of first and second devices, said first drain terminal [[being]]is connected to said second drain terminal via the multi-layer metal interconnect structure, and said first gate terminal [[being]]is connected to said second gate terminal via the multi-layer metal interconnect structure, ~~wherein~~ (ii) said first and second gate terminals of the first pair of power transistor devices are electrically independent of the first and second gate terminals of the second pair of power transistor devices, (iii) said first and second drain terminals of the first pair of devices are electrically independent of the first and second drain terminals of the second pair of devices, ([[iii]]iv)

the multi-layer metal interconnect structure includes a first electrically isolated lead ~~comprises~~comprising both first source terminals connected to both second source terminal, ([[i]]v) the multi-layer metal interconnect structure includes a second electrically isolated lead ~~comprises~~comprising said first and second drain terminals of the first pair of power transistor devices, (vi) the multi-layer metal interconnect structure includes a third electrically isolated lead ~~comprises~~comprising said first and second drain terminals of the second pair of power transistor devices, (vii) the multi-layer interconnect structure includes a fourth electrically isolated lead ~~comprises~~comprising said first and second gate terminals of the first pair of power transistor devices, and (viii) the multi-layer metal interconnect structure includes a fifth electrically isolated lead comprising said first and second gate terminals of the second pair of power transistor devices.

14. (Previously presented) The monolithic structure of claim 13 wherein each of said first and second lateral power transistor devices comprises a lateral power MOSFET.

15. (Previously presented) The monolithic structure of claim 13 wherein a size of said second lateral power transistor is smaller than a size of said first lateral power transistor.

16. (Previously presented) The monolithic structure of claim 13 wherein a first threshold voltage of said first lateral power transistor is different from a second threshold voltage of said second lateral power transistor, and a difference in threshold voltages is at least approximately 0.1 V.

17. (New) The monolithic structure of claim 1, wherein each of the first and second lateral devices comprise source and drain dopants of a same type.

18. (New) The monolithic structure of claim 7, wherein each of the first and second lateral devices comprise source and drain dopants of a same type.

19. (New) The monolithic structure of claim 9, wherein each of the first and second lateral devices comprise source and drain dopants of a same type.

20. (New) The monolithic structure of claim 13, wherein each of the first and second lateral devices comprise source and drain dopants of a same type.